REMARKS

This Amendment is filed in response to the Office Action dated August 24, 2006, which has a shortened statutory period set to expire November 24, 2006.

Allowable Subject Matter

Applicant greatly appreciates the Examiner's indication of allowable subject matter. Specifically, Claim 73 is objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant notes that Claim 73 depends from Claim 68, which Applicant believes to be patentable over the cited references. Therefore, Applicant has not amended Claim 73 herein.

Claims 37-39 And 49-51 Are Patentable Over Rompaey, Cadence, And Hellestrand

Claim 37 recites in part (emphasis added):

> responsive to a second sequence of user commands, forming a virtual embedded system including an instruction set accurate simulator of a target processor core and coupling read, write, and interrupt signals of the instruction set accurate simulator with an FSM simulation of at least one hardware element, wherein generating said FSM simulation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol; ... and
>
> responsive to a user request, displaying on the GUI a graphical representation of the execution of the software application on the virtual embedded system that includes a software debugger interface to debug the loaded software and a virtual test-bench associated with the GUI and adapted to interact with the simulation, wherein the virtual test-bench is created using a test-bench builder for generating a

graphical representation of at least one interactive test-bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test-bench, to emulate user input to and device output from the virtual embedded system.

Applicant respectfully submits that the cited references fail to disclose or suggest these limitations. For example, Rompaey teaches a hardware/software co-design environment that allows specifying, simulating, and synthesizing heterogeneous hardware/software architectures from a heterogeneous specification. Col. 7, lines 31-35. This environment is based on encapsulating existing hardware and software compilers and allows for the interactive synthesis of hardware/software as well as hardware/hardware interfaces. Col. 7, lines 35-39.

The Final Office Action cites the following passages of Rompaey as teaching forming the virtual embedded system: col. 9, lines 19-22; col. 20, line 55 to col. 21, line 14; and col. 11, lines 5-6. Applicant respectfully traverses this characterization. Col. 9, lines 19-22 teach that a hybrid simulation includes both hardware implementations and computer simulations, wherein the hardware implementation can include hardware and software subsystems (the software subsystems being executed on the hardware subsystems). This simulation has nothing to do with an FSM, much less the recited generating of the FSM simulation. Col. 20, line 55 to col. 21, line 14 teach that the ports 75 of the software model 71 (see FIG. 7) for an ARM processor have primitive protocols, wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. This software model has nothing to do with an FSM, much less the recited generating of the FSM simulation. Col. 11, lines 5-6 teach that FIG. 11 is a schematic representation of a pager

application. FIG. 11 shows Remote Procedure Call (RPC) communication for the pager design. Col. 24, lines 50-51. In this RPC communication, blocks 91-101 correspond to processes 89 (i.e. tracking and acquisition, frame extraction, correlator and noise estimator, and user interface) shown in FIG. 10. Col. 24, lines 51-53. However, these blocks have nothing to do with an FSM, much less the recited generating of the FSM simulation.

Thus, Applicant respectfully submits that these cited passages of Rompaey fail to disclose or suggest the recited step of forming the virtual embedded system including an instruction set accurate simulator of a target processor core and coupling read, write, and interrupt signals of the instruction set accurate simulator with an FSM simulation of at least one hardware element, wherein generating said FSM simulation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol.

The Final Office Action admits that Rompaey does not disclose or suggest the recited step of displaying. Applicant agrees with this characterization. However, the Final Office Action cites Hellestrand (col. 21, lines 39-59) or, alternatively, Cadence (page 2, paragraphs 1-3) as teaching the recited displaying. Applicant respectfully traverses these characterizations. Col. 21, lines 39-59 (Hellestrand) teach that prior to execution, a user can insert, enable, or disable debugger breakpoints in the user programs for each processor simulator. During simulation, when a breakpoint is encountered, the debugger stops, thereby allowing any software variable in any processor simulator and any hardware variable in the

hardware simulator to be examined by a user. Page 2, paragraphs 1-3 (Cadence) states that the Interactive Simulation Library™ (ISL), which is a library provided by Cadence, allows the control and monitoring of multiple inputs/outputs and design parameters to facilitate the testing of virtual test instruments (e.g. oscilloscopes, spectrum analyzers, and signal generators).

Applicant respectfully submits that neither reference, i.e. Hellestrand or Cadence, teaches the recited step of displaying on the GUI a graphical representation of the execution of the software application on the virtual embedded system that includes a software debugger interface to debug the loaded software and a virtual test-bench associated with the GUI and adapted to interact with the simulation, wherein the virtual test-bench is created using a test-bench builder for generating a graphical representation of at least one interactive test-bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test-bench, to emulate user input to and device output from the virtual embedded system.

Therefore, even when Rompaey, Hellestrand, and Cadence are combined (assuming these references can be combined, which is not conceded herein), the recited steps of forming a virtual embedded system and displaying are still neither disclosed nor suggested. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 37.

Claims 38-39 and 49-51 depend from Claim 37 and therefore are patentable for at least the reasons presented for Claim 37. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 38-39 and 49-51.

Claims 40-42 Are Patentable Over Rompaey, Cadence, Hellestrand, And Schwab

Claims 40-42 depend from Claim 37 and therefore are patentable for at least the reasons presented for Claim 37. Schwab fails to remedy the deficiency of Rompaey, Cadence, and Hellestrand with respect to Claim 37. Specifically, Schwab teaches an interactive secure identification transaction system for storing, retrieving, and displaying text and data compressed image files and communicating those between a centralized server computer and a plurality of client data terminals located at remote sites. Paragraph [0002]. Applicant submits that Schwab teaches nothing about an FSM or FSM simulation, much less the recited steps of forming a virtual embedded system or displaying. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 40-42.

Claims 43-48 Are Patentable Over Rompaey, Cadence, Hellestrand, And Van Huben

Claims 43-48 depend from Claim 37 and therefore are patentable for at least the reasons presented for Claim 37. Van Huben fails to remedy the deficiency of Rompaey, Cadence, and Hellestrand with respect to Claim 37. Specifically, Van Huben teaches storing, moving, retrieving and managing data in a system comprised of one or more shared public libraries interacting with one or more private libraries arranged in a client server environment. Col. 6, line 65 to col. 7, line 1. Therefore, Applicant submits that Van Huben teaches nothing about an FSM or FSM simulation, much less the recited steps of forming a virtual embedded system or displaying. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 43-48.

Claims 52-59, 64, And 89 Are Patentable Over Rompaey And Cadence

Claim 52 recites in part (emphasis added):

generating a virtual hardware component that is a finite state machine (FSM) representation of at least one hardware component, said generating comprising applying a design language having at least one graphical symbol and adapted to form an FSM representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol; [and]

linking read, write, and interrupt signals of the instruction set accurate simulator of the target processor core with corresponding signals of the at least one virtual hardware component to form a virtual embedded system.

Applicant respectfully submits that the cited references fail to disclose or suggest these limitations. For example, Rompaey teaches a hardware/software co-design environment that allows specifying, simulating, and synthesizing heterogeneous hardware/software architectures from a heterogeneous specification. Col. 7, lines 31-35. This environment is based on encapsulating existing hardware and software compilers and allows for the interactive synthesis of hardware/software as well as hardware/hardware interfaces. Col. 7, lines 35-39.

The Final Office Action cites the following passages of Rompaey as teaching generating the virtual hardware component that is a FSM representation: col. 9, lines 19-22; col. 20, line 55 to col. 21, line 14; and col. 11, lines 5-6. Applicant respectfully traverses this characterization. Col. 9, lines 19-22 teach that a hybrid simulation includes both hardware implementations and computer simulations, wherein the hardware implementation can include hardware and software subsystems (the software subsystems being executed on the hardware subsystems). This hybrid simulation has nothing to do with an FSM, much less the recited generating of the virtual hardware component that is an FSM representation of at least one hardware component. Col. 20, line 55 to col. 21, line 14 teach that the ports 75 of the

software model 71 (see FIG. 7) have primitive protocols, wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. This software model has nothing to do with an FSM, much less the recited generating of the virtual hardware component that is an FSM representation of at least one hardware component. Col. 11, lines 5-6 teach FIG. 11 is a schematic representation of a pager application. FIG. 11 shows Remote Procedure Call (RPC) communication for the pager design. Col. 24, lines 50-51. In this RPC communication, blocks 91-101 correspond to processes 89 (i.e. tracking and acquisition, frame extraction, correlator and noise estimator, and user interface) shown in FIG. 10. Col. 24, lines 51-53. However, these blocks have nothing to do with an FSM, much less the recited generating of the virtual hardware component that is an FSM representation of at least one hardware component.

Thus, Applicant respectfully submits that these cited passages of Rompaey fail to disclose or suggest the recited step of generating the virtual hardware component that is a finite state machine (FSM) representation of at least one hardware component, the generating comprising applying a design language having at least one graphical symbol and adapted to form an FSM representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol.

The Final Office Action cites col. 9, lines 19-22 and col. 20, line 55 to col. 21, line 14 of Rompaey as teaching linking read, write, and interrupt signals of the instruction set accurate simulator of the target processor core with corresponding signals of the at least one virtual hardware component to form a virtual embedded system. Applicant

respectfully traverses this characterization. As noted above, this passage teaches that the ports 75 of the software model 71 (see FIG. 7) have primitive protocols, wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. Merely providing ports does not teach linking the recited signals to form the virtual embedded system. Therefore, Applicant submits that Rompaey also fails to disclose or suggest the recited linking step.

Applicant respectfully submits that Cadence fails to remedy the deficiency of Rompaey with respect to Claim 52. Specifically, Cadence fails to disclose or suggest the recited steps of generating the virtual hardware component and linking read, write, and interrupt signals.

Therefore, even when Rompaey and Cadence are combined (assuming these references can be combined, which is not conceded herein), the recited steps of generating the virtual hardware component and linking read, write, and interrupt signals are still neither disclosed nor suggested. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 52.

Claims 53-59 depend from Claim 52 and therefore are patentable for at least the reasons presented for Claim 52. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 53-59.

Claim 64 recites in part (emphasis added):

> generating a finite state machine (FSM) representation of at least one hardware element, said generating comprising applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol;

designing a virtual prototype of the embedded system having an instruction set accurate simulator of a processor core and coupling read, write, and interrupt signals of the instruction set accurate simulator with said FSM representation of at least one hardware element; [and]

creating a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench.

Applicant respectfully submits that the cited references fail to disclose or suggest these limitations. For example, Rompaey teaches a hardware/software co-design environment that allows specifying, simulating, and synthesizing heterogeneous hardware/software architectures from a heterogeneous specification. Col. 7, lines 31-35. This environment is based on encapsulating existing hardware and software compilers and allows for the interactive synthesis of hardware/software as well as hardware/hardware interfaces. Col. 7, lines 35-39.

The Final Office Action cites the following passages of Rompaey as teaching generating a FSM representation of at least one hardware element: col. 9, lines 19-22; col. 20, line 55 to col. 21, line 14; and col. 11, lines 5-6. Applicant respectfully traverses this characterization. Col. 9, lines 19-22 teach that a hybrid simulation includes both hardware implementations and computer simulations, wherein the hardware implementation can include hardware and software subsystems (the software subsystems being executed on the hardware subsystems). This simulation has nothing to do with an FSM, much less the recited generating of the FSM representation of at least one hardware element. Col. 20, line 55 to col. 21, line 14 teach

that the ports 75 of the software model 71 (see FIG. 7) have primitive protocols, wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. This software model has nothing to do with an FSM, much less the recited generating of the FSM representation of at least one hardware element. Col. 11, lines 5-6 teach FIG. 11 is a schematic representation of a pager application. FIG. 11 shows Remote Procedure Call (RPC) communication for the pager design. Col. 24, lines 50-51. In this RPC communication, blocks 91-101 correspond to processes 89 (i.e. tracking and acquisition, frame extraction, correlator and noise estimator, and user interface) shown in FIG. 10. Col. 24, lines 51-53. However, these blocks have nothing to do with an FSM, much less the recited generating of the FSM representation of at least one hardware element.

Applicant respectfully submits that these cited passages of Rompaey fail to disclose or suggest the recited step of generating the FSM representation of at least one hardware element, the generating comprising applying a design language having at least one graphical symbol and adapted to form an FSM representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol.

The Final Office Action cites col. 20, line 55 to col. 21, line 14 of Rompaey as teaching designing the virtual prototype of the embedded system. Applicant respectfully traverses this characterization. As noted above, this passage teaches that the ports 75 of the software model 71 (see FIG. 7) have primitive protocols, wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. Merely providing ports does

not teach designing a virtual prototype of the embedded system having an instruction set accurate simulator of a processor core and coupling read, write, and interrupt signals of the instruction set accurate simulator with said FSM representation of at least one hardware element. Therefore, Applicant submits that Rompaey also fails to disclose or suggest the recited designing step.

The Final Office Action admits that Rompaey fails to disclose or suggest the step of creating the virtual test bench. Applicant agrees with this characterization. However, the Final Office Action then cites Cadence, page 2, paragraphs 1-3 as teaching this step. Applicant respectfully traverses this characterization. Specifically, Cadence fails to disclose or suggest a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench.

Therefore, even when Rompaey and Cadence are combined (assuming these references can be combined, which is not conceded herein), the recited steps of generating the FSM representation, designing the virtual prototype, and creating the virtual test bench are still neither disclosed nor suggested. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 64.

Claim 89 depends from Claim 64 and therefore is patentable for at least the reasons presented for Claim 64. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 89.

Claims 60-63 Are Patentable Over Rompaey, Cadence, And Van Huben

Claims 60-63 depend from Claim 52 and therefore are patentable for at least the reasons presented for Claim 52. Van

Huben fails to remedy the deficiency of Rompaey and Cadence with respect to Claim 52. Specifically, Van Huben teaches storing, moving, retrieving and managing data in a system comprised of one or more shared public libraries interacting with one or more private libraries arranged in a client server environment. Col. 6, line 65 to col. 7, line 1. Therefore, Applicant submits that Van Huben teaches nothing about the recited steps of generating the virtual hardware component and linking read, write, and interrupt signals. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 60-63.

Claims 65-67 Are Patentable Over Rompaey, Cadence, And Schubert

Claims 65-67 depend from Claim 64 and therefore are patentable for at least the reasons presented for Claim 64. Schubert fails to remedy the deficiency of Rompaey and Cadence with respect to Claim 64. Specifically, Schubert teaches techniques and systems for analysis, diagnosis and debugging fabricated hardware designs at a Hardware Description Language (HDL) level. Paragraph [0024]. However, Schubert teaches nothing about designing a virtual prototype or creating the virtual test bench. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 65-67.

Claims 68-70 Are Patentable Over Rompaey, Cadence, And Van Huben

Claim 68 recites in part (emphasis added):

> designing a virtual prototype of the embedded system, the virtual prototype having an instruction set accurate simulator of a target processor core and a finite state machine (FSM) representation of a hardware element within the embedded system, the FSM representation configured to couple memory read/write requests and interrupt signals with the instruction

set accurate simulator of the target processor core, wherein generating said FSM representation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol;

creating a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench.

Applicant respectfully submits that the cited references fail to disclose or suggest these limitations. For example, Rompaey teaches a hardware/software co-design environment that allows specifying, simulating, and synthesizing heterogeneous hardware/software architectures from a heterogeneous specification. Col. 7, lines 31-35. This environment is based on encapsulating existing hardware and software compilers and allows for the interactive synthesis of hardware/software as well as hardware/hardware interfaces. Col. 7, lines 35-39.

The Final Office Action cites FIG. 11 and the following passages of Rompaey as teaching forming the virtual prototype of the embedded system: col. 20, line 55 to col. 21, line 14; and col. 11, lines 5-6. Applicant respectfully traverses this characterization. Col. 20, line 55 to col. 21, line 14 teach that the ports 75 of the software model 71 (see FIG. 7) have primitive protocols, wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. This software model has nothing to do with an FSM, much less the recited FSM representation configured to couple requests and interrupt

signals with the instruction set accurate simulator. Col. 11, lines 5-6 teach FIG. 11 is a schematic representation of a pager application. FIG. 11 shows Remote Procedure Call (RPC) communication for the pager design. Col. 24, lines 50-51. In this RPC communication, blocks 91-101 correspond to processes 89 (i.e. tracking and acquisition, frame extraction, correlator and noise estimator, and user interface) shown in FIG. 10. Col. 24, lines 51-53. However, these blocks have nothing to do with an FSM, much less the recited FSM representation configured to couple requests and interrupt signals with the instruction set accurate simulator.

Applicant respectfully submits that FIG. 11 and these cited passages of Rompaey fail to disclose or suggest the recited step of designing a virtual prototype of the embedded system, the virtual prototype having an instruction set accurate simulator of a target processor core and a finite state machine (FSM) representation of a hardware element within the embedded system, the FSM representation configured to couple memory read/write requests and interrupt signals with the instruction set accurate simulator of the target processor core, wherein generating said FSM representation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-definable textual portion defining the behavior of the graphical symbol.

The Final Office Action admits that Rompaey does not disclose or suggest the recited step of creating a virtual test bench. Applicant agrees with this characterization. However, the Final Office Action then cites Cadence (page 2, paragraphs 1-3) as teaching the recited step of creating. Applicant respectfully traverses these characterizations. Page 2,

paragraphs 1-3 (Cadence) states that the Interactive Simulation Library™ (ISL), which is a library provided by Cadence, allows the control and monitoring of multiple inputs/outputs and design parameters to facilitate the testing of virtual test instruments (e.g. oscilloscopes, spectrum analyzers, and signal generators).

Thus, Applicant respectfully submits that Cadence does not teach the recited step of creating a virtual test bench having a graphical representation of a human/machine interface for interacting with the embedded system using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for each interactive test bench.

Van Huben fails to remedy the deficiency of Rompaey and Cadence with respect to Claim 68. Specifically, Van Huben teaches storing, moving, retrieving and managing data in a system comprised of one or more shared public libraries interacting with one or more private libraries arranged in a client server environment. Col. 6, line 65 to col. 7, line 1. Therefore, Applicant submits that Van Huben teaches nothing about the recited steps of designing a virtual prototype of the embedded system or creating a virtual test bench.

Therefore, even when Rompaey, Cadence, and Van Huben are combined (assuming these references can be combined, which is not conceded herein), the recited steps of designing a virtual prototype of the embedded system and creating a virtual test bench are still neither disclosed nor suggested. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 68.

Claims 69-70 depend from Claim 68 and therefore are patentable for at least the reasons presented for Claim 68.

Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 69-70.

Claims 71-72 Are Patentable Over Rompaey, Cadence, Van Huben, And Schwab

Claims 71-72 depend from Claim 68 and therefore are patentable for at least the reasons presented for Claim 68. Schwab fails to remedy the deficiency of Rompaey, Cadence, and Van Huben with respect to Claim 68. Specifically, Schwab teaches an interactive secure identification transaction system for storing, retrieving, and displaying text and data compressed image files and communicating those between a centralized server computer and a plurality of client data terminals located at remote sites. Paragraph [0002]. Applicant submits that Schwab teaches nothing about an FSM, much less the recited steps of designing a virtual prototype of the embedded system or creating a virtual test bench. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 71-72.

Claims 74 And 76-78 Are Patentable Over Van Huben, Rompaey, And Cadence

Claim 74 recites in part (emphasis added):

> accessing a database of virtual prototypes of embedded systems, each of the virtual prototypes having a processor simulator, a finite state machine (FSM) representation of hardware peripherals, and a virtual test bench emulating a human/machine interface for interacting with a simulation of the operation of the virtual prototype,
>
> wherein generating said FSM representation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, each graphical symbol of the design language having a graphical portion and a user-

definable textual portion defining the behavior of the graphical symbol, and

wherein the virtual test bench is created using a test bench builder for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for the interactive test bench.

Applicant respectfully submits that the cited references fail to disclose or suggest these limitations. For example, Rompaey teaches a hardware/software co-design environment that allows specifying, simulating, and synthesizing heterogeneous hardware/software architectures from a heterogeneous specification. Col. 7, lines 31-35. This environment is based on encapsulating existing hardware and software compilers and allows for the interactive synthesis of hardware/software as well as hardware/hardware interfaces. Col. 7, lines 35-39.

The Final Office Action cites the following passages of Rompaey as teaching accessing a database of virtual prototypes of embedded systems: col. 9, lines 19-22; col. 13, lines 39-48; col. 20, line 55 to col. 21, line 14; and col. 11, lines 5-6. Applicant respectfully traverses this characterization. Col. 9, lines 19-22 teach a heterogeneous implementation comprising hardware subsystems and software subsystems, wherein the software subsystems can be executed on one or more hardware subsystems. This passage teaches nothing about each virtual prototype having an FSM representation of hardware peripherals. Col. 13, lines 39-48 teach an interface synthesis whereby each communication channel is refined by selection of a communication scenario. This passage also teaches nothing about each virtual prototype having an FSM representation of hardware peripherals. Col. 20, line 55 to col. 21, line 14 teach that the ports 75 of the software model 71 (see FIG. 7) have primitive protocols,

wherein the software model contains a behavioral description that allows compiling a software host language encapsulation into machine code. This software model has nothing to do with an FSM, much less the recited FSM representation of hardware peripherals. Col. 11, lines 5-6 teach FIG. 11 is a schematic representation of a pager application. FIG. 11 shows Remote Procedure Call (RPC) communication for the pager design. Col. 24, lines 50-51. In this RPC communication, blocks 91-101 correspond to processes 89 (i.e. tracking and acquisition, frame extraction, correlator and noise estimator, and user interface) shown in FIG. 10. Col. 24, lines 51-53. However, these blocks have nothing to do with an FSM, much less the recited FSM representation of hardware peripherals.

Applicant respectfully submits that these cited passages of Rompaey fail to disclose or suggest the recited step of accessing a database of virtual prototypes of embedded systems, each of the virtual prototypes having a … a finite state machine (FSM) representation of hardware peripherals, … wherein generating said FSM representation comprises applying a design language having at least one graphical symbol and adapted to form a finite state machine representation of electronic hardware, … wherein the virtual test bench is created using a test bench builder for … selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for the interactive test bench.

The Final Office Action cites Cadence (page 2, paragraphs 1-3) as teaching the recited virtual test bench. Applicant respectfully traverses this characterization. Page 2, paragraphs 1-3 (Cadence) states that the Interactive Simulation Library™ (ISL), which is a library provided by Cadence, allows the control and monitoring of multiple inputs/outputs and design

parameters to facilitate the testing of virtual test instruments (e.g. oscilloscopes, spectrum analyzers, and signal generators).

Thus, Applicant respectfully submits that Cadence does not teach the recited virtual test bench for generating a graphical representation of at least one interactive test bench and for selecting signals or variables associated with the FSM and to be coupled to a graphical representation of a user interface for the interactive test bench.

Van Huben fails to remedy the deficiency of Rompaey and Cadence with respect to Claim 74. Specifically, Van Huben teaches storing, moving, retrieving and managing data in a system comprised of one or more shared public libraries interacting with one or more private libraries arranged in a client server environment. Col. 6, line 65 to col. 7, line 1. Therefore, Applicant submits that Van Huben teaches nothing about the recited virtual prototypes, each having an FSM representation of hardware peripherals.

Therefore, even when Rompaey, Cadence, and Van Huben are combined (assuming these references can be combined, which is not conceded herein), the recited accessing of the database of virtual prototypes of embedded systems is still neither disclosed nor suggested. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 74.

Claims 76-78 depend from Claim 74 and therefore are patentable for at least the reasons presented for Claim 74. Based on those reasons, Applicant requests reconsideration and withdrawal of the rejection of Claims 76-78.

Claim 75 Is Patentable Over Van Huben, Rompaey, Cadence, And Schwab

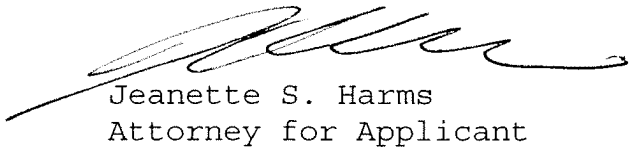
Claim 75 depends from Claim 74 and therefore is patentable for at least the reasons presented for Claim 74. Schwab fails to remedy the deficiency of Van Huben, Rompaey, and Cadence with respect to Claim 74. Specifically, Schwab teaches an interactive secure identification transaction system for storing, retrieving, and displaying text and data compressed image files and communicating those between a centralized server computer and a plurality of client data terminals located at remote sites. Paragraph [0002]. Applicant submits that Schwab teaches nothing about an FSM representation of hardware peripherals. Based on the above reasons, Applicant requests reconsideration and withdrawal of the rejection of Claim 75.

CONCLUSION

Claims 37-78 and 89 are pending in the present application. Allowance of these claims is respectfully requested.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,



Customer No.: 35273

Jeanette S. Harms
Attorney for Applicant
Reg. No. 35,537